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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,741	09/22/2005	Radu Catalin Surdeanu	NL03 0347 US1	6084

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EXAMINER	
LIN, JOHN	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/550,741	SURDEANU ET AL.	
	Examiner	Art Unit	
	JOHN LIN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-14 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-14 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-14 and 17-23 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites, "a gate electrode formed on a gate insulating film" and claim 13 recites, "a gate insulator is provided between the semiconductor substrate and the gate electrode." It is unclear and indefinite as to whether the gate insulating film claimed in claim 1 and the gate insulator claimed in claim 13 are the same. For the purpose of applying art, it will be interpreted to be the same element.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7, 9, 10-14, 17 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. PGPUB 2003/0049919, granted to "**Yamamoto**" in view of U.S. Patent 6,399,515, granted to "**Tao**."

Claims 6, 7 and 17: Yamamoto discloses an MIS type semiconductor device, Fig. 5, comprising:

a semiconductor substrate (1),

a gate electrode (73 and 75) formed on a gate insulating film (6) and formed of gate material,

wherein the gate electrode comprises:

a first layer of activated crystalline gate material (73) having a first side oriented towards the substrate, a second side oriented away from the substrate and a grain size, and

a second layer of gate material (75) at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the second layer of gate material is at least twice as large as the grain size of the first layer of activated crystalline gate material (paragraphs [0044], [0046], [0049-0052], [0060], and [0079]).

Yamamoto appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^9 ions/cm^3 (claim 6), 10^{20} ions/cm^3 (claim 7), $5x10^{20}$ ions/cm^3 (claim 17) or higher.

Tao, however, discloses a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Yamamoto so the first layer of activated crystalline gate material has a doping level greater than 10^{20} ions/cm^3.

Claim 9: Yamamoto discloses the second layer of gate material (75) consists of amorphous gate material (paragraph [0060]).

Claim 10: Yamamoto discloses the second layer of gate material (75) consists of polycrystalline gate material (paragraph [0060]).

Claims 11 and 12: Yamamoto in view of Tao appears not to explicitly disclose the grain size in the second layer is below about 40 nm, and the first layer is crystalline or very fine-grained with grains below 5 nm.

Grain size is a result-affecting parameter because the grain size affects the conductivity of the layer.

According to well-established patent law precedents (see, for example M.P.E.P. § 2144.05) therefore it would have been obvious to optimize (for example by routine experimentation) the grain sizes of the first and second layers.

Claim 13: Yamamoto discloses a gate insulator (6) is provided between the semiconductor substrate and the gate electrode (Fig. 5; paragraph [0046]).

Claim 14: Yamamoto the device is a transistor (Fig. 5).

Claim 20: Yamamoto in view of Tao appears not to explicitly disclose the grain size in the second layer is below about 30 nm.

Grain size is a result-affecting parameter because the grain size affects the conductivity of the layer.

According to well-established patent law precedents (see, for example M.P.E.P. § 2144.05) therefore it would have been obvious to optimize (for example by routine experimentation) the grain sizes of the second layer.

Claim 21: Yamamoto discloses the grain size of the second layer of gate material is about six times as large as the grain size of the first layer of activated crystalline gate material (paragraphs [0060] and [0079]).

Claim 22: The recitation "the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film" has been considered and determined to be functional language, making the claim scope not distinguish over a layer of activated crystalline gate material capable of having grain size to reduce gaps between a layer of activated crystalline gate material and a gate insulting film. The claim recitations do not require the grain size of the first layer of activated crystalline gate material reduces gaps between the first layer of activated crystalline gate material and the gate insulating film to be part of the elements limiting the claim scope. See MPEP § 2114, and precedents cited therein.

Claim 23: Yamamoto discloses the first layer (73) of activated crystalline gate material is silicon (Fig. 5).

Claim 24: Yamamoto discloses an MIS type semiconductor device, in Fig. 5, comprising:

a semiconductor substrate (1);

a gate insulating film (6) formed on the substrate; and

a gate electrode (73 and 75) formed on the gate insulating film, the gate electrode including:

a first layer (73) of activated crystalline gate material having a first side oriented towards the substrate, a second side oriented away from the substrate, and

a second layer (75) of gate material at the second side of the first layer of activated crystalline gate material,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material (paragraphs [0044], [0046], [0049-0052], [0060], and [0079]).

Yamamoto appears not to explicitly disclose the first layer of activated crystalline gate material having a doping level of 10^9 ions/cm^3 or higher.

Tao, however, discloses a gate electrode doped to a level greater than about 10^{20} dopant atoms per cubic centimeter in order to assure optimal conductivity (column 9, lines 14-37).

To assure optimal conductivity therefore it would have been obvious to modify Yamamoto so the first layer of activated crystalline gate material has a doping level of 10^9 ions/cm^3 or higher.

Yamamoto in view of Tao appears not to explicitly disclose the grain size in the first layer having a grain size of less than about 5nm, and second layer having a grain size of less than about 40 nm.

Grain size is a result-affecting parameter because the grain size affects the conductivity of the layer.

According to well-established patent law precedents (see, for example M.P.E.P. § 2144.05) therefore it would have been obvious to optimize (for example by routine experimentation) the grain sizes of the first and second layers.

Claims 8, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Tao as applied to claims 6, 7, 9, 10-14, 17 and 20-24 above, and further in view of U.S. Patent 6,172,399, granted to "**Lee**."

Claims 8, 18 and 19: Yamamoto in view of Tao discloses all the limitations of claim of claim 6. Yamamoto in view of Tao appears not to explicitly disclose the doping implant in the activated gate material has an abruptness of about 2nm or more (claim 8); about 1.5nm (claim 18) or more; or about 1nm (claim 19).

Lee, however, discloses and motivates a profile abruptness less than 10nm per order of magnitude charge in dopant concentration in order to have better threshold voltage roll-off characteristics (column 1, lines 54-58).

To have better threshold voltage roll-off characteristics therefore it would have been obvious to modify Yamamoto to have a doping implant in the activated gate material have an abruptness of a doping profile of about 10nm or less.

Also, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's arguments with respect to claims 6-14 and 17-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

A shortened statutory period for reply to this Office Action is set to expire THREE MONTHS from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LIN whose telephone number is (571)270-1274. The examiner can normally be reached on M-F, 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815

/J. L./
Examiner, Art Unit 2815